

Application Serial No. 10/750580  
Amendment dated March 10, 2006  
Reply to Office Action dated December 12, 2005

Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently Amended) An integrated package comprising:
  - a first wafer having a first surface;
  - a second wafer having a first surface bonded at a first perimeter to the first surface of the first wafer; and
  - a recess formed in the first surface of the first wafer between the first perimeter and in a second perimeter situated within the first perimeter for a window situated within the second perimeter.
2. (Previously presented) The package of claim 1, further comprising a first bump pattern in the first surface of the first wafer within the second perimeter.
3. (Previously presented) The package of claim 2, further comprising a second bump pattern on a second surface of the first wafer.

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4. (Previously presented) The package of claim 3, further comprising a seal between the first and second wafers at the first perimeter.

5. (Previously presented) The package of claim 4, wherein the seal comprises:

a spacer material; and  
a layer of malleable material.

6. (Previously presented) The package of claim 5, wherein the seal further comprises a layer of bondable material.

7. (Previously presented) The package of claim 6, further comprising structural supports in the recess of the first wafer.

8. (Previously presented) The package of claim 7, further comprising at least one pumpout opening in the first wafer.

9. (Previously presented) The package of claim 8, wherein the first and second wafers comprise silicon.

10-25. (Canceled)

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26. (Withdrawn) An integral package comprising:

    a first wafer comprising:

        a seal along a first perimeter on a first surface of the first wafer; and

        a trench in the first surface of the first wafer along a second perimeter within the first perimeter; and

    a second wafer having a first surface bonded to the first wafer along the seal.

27. (Withdrawn) The package of claim 26, wherein the first wafer further comprises an anti-reflective pattern on the first surface.

28. (Withdrawn) The package of claim 27, wherein the first wafer further comprises at least one vent hole and vent hole seal.

29. (Withdrawn) The package of claim 28, wherein the seal comprises a spacer material.

30. (Withdrawn) The package of claim 29, wherein the first wafer further comprises an anti-reflective pattern on a second surface.

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31. (New) An integrated package comprising:

    a first wafer having a first surface;

    a second wafer having a first surface bonded at a first perimeter to the first surface of the first wafer;

    a recess formed in the first surface of the first wafer in a second perimeter situated within the first perimeter;

    structural supports in the recess of the first wafer;

    a first bump pattern in the first surface of the first wafer within the second perimeter;

    a second bump pattern on a second surface of the first wafer; and

    a seal between the first and second wafers at the first perimeter; and

    wherein the seal comprises:

        a spacer material;

        a layer of malleable material; and

        a layer of bondable material.

32. (New) The package of claim 31, further comprising at least one pumpout opening in the first wafer.

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33. (New) The package of claim 32, wherein the first and second wafers comprise silicon.

34. (New) An integrated package comprising:  
a first wafer having a first surface;  
a second wafer having a first surface bonded at a first perimeter to the first surface of the first wafer;  
a recess formed in the first surface of the first wafer in a second perimeter situated within the first perimeter; and  
structural supports in the recess of the first wafer;

35. (New) The package of claim 34, further comprising a seal between the first and second wafers at the first perimeter.

36. (New) The package of claim 35, further comprising at least one pumpout opening in the first wafer.

37. (New) The package of claim 36, further comprising a first bump pattern in the first surface of the first wafer within the second perimeter.

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38. (New) The package of claim 37, further comprising a second bump pattern on a second surface of the first wafer.

39. (New) The package of claim 38, wherein the first and second wafers comprise silicon.

40. (New) An integrated package comprising:  
a first wafer having a first surface;  
a second wafer having a first surface bonded at a first perimeter to the first surface of the first wafer;  
a recess formed in the first surface of the first wafer in a second perimeter situated within the first perimeter; and  
a first bump pattern on a second surface of the first wafer.

41. (New) The package of claim 40, further comprising a seal between the first and second wafers at the first perimeter.

42. (New) The package of claim 41, further comprising structural supports in the recess of the first wafer.

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43. (New) The package of claim 42, further comprising at least one pumpout opening in the first wafer.

44. (New) The package of claim 43 a second bump pattern on a first surface of the first wafer.

45. (New) The package of claim 44, wherein the first and second wafers comprise silicon.

46. (New) An integrated package comprising:  
a first wafer having a first surface;  
a second wafer having a first surface bonded at a first perimeter to the first surface of the first wafer;  
a recess formed in the first surface of the first wafer between the first perimeter and a second perimeter situated within the first perimeter for a window situated within the second perimeter;  
and  
at least one pumpout opening in the first wafer.

47. (New) The package of claim 46, further comprising structural supports in the recess of the first wafer.

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48. (New) The package of claim 47, further comprising a first bump pattern in the first surface of the first wafer within the second perimeter.

49. (New) The package of claim 48, further comprising a second bump pattern on a second surface of the first wafer.

50. (New) The package of claim 49, further comprising a seal between the first and second wafers at the first perimeter.

51. (New) The package of claim 50, wherein the first and second wafers comprise silicon.